IN THE CLAIMS

1-9. (Canceled)

10. (Currently Amended) A switch comprising:

a plurality of serial input ports coupled to a first bus;

a memory coupled to the input ports; and

a plurality of serial output ports coupled to the memory and to a second bus, wherein each serial input port and each serial output port are coupled to a programmable counter having programmable start and stop values , the programmable counter operable to increment the start value until the start value reaches a maximum count at which time the programmable counter rolls the start value over to a starting count and continues to increment the start value.

11. (Original) The switch of claim 10, and further comprising:

a parity generator coupled between the serial input ports and the memory; and

a parity checker coupled between the memory and the serial output ports.

12. (Original) The switch of claim 10 wherein each of the serial input and serial output ports are double buffered.

13. (Original) The switch of claim 10 and further comprising:

a controller coupled to the switch for controlling routing of ATM cells of data between the serial input ports and the serial output ports.

14. (Original) An ATM switch comprising:

a plurality of serial input ports coupled to a first bus;

a memory coupled to the input ports; and

a plurality of serial output ports coupled to the memory and to a second bus, wherein each serial input port and each serial output port are coupled to a programmable counter comprising:

multiple latches for providing a count output;
a start count circuit coupled to the latches;
a stop count circuit coupled to said latches;
a maximum count circuit coupled to the latches; and
a compare circuit coupled to the stop count circuit and the latches.

15. (Original) The ATM switch of claim 14 and further comprising a controller coupled to the switch for controlling routing of ATM cells of data between serial input ports and serial output ports.

16. (Original) The ATM switch of claim 14, and further comprising:
a parity generator coupled between the serial input ports and the memory; and
a parity checker coupled between the memory and the serial output ports.

17. (Original) The ATM switch of claim 14, wherein each of the serial input ports and the serial output ports are double buffered.

18. (Currently Amended) A switch comprising:
a plurality of input ports coupled to a first bus;
a memory coupled to the input ports; ~~and~~
a plurality of output ports coupled to the memory and to a second bus, wherein each input port and each output port are coupled to a programmable counter having programmable start and stop values , the programmable counter having a start count and a maximum count and is programmed to increment the start value until the start value reaches the maximum count at which time the counter rolls over to the start count and continues to increment the start value until it reaches the stop value.

19. (Previously Presented) An ATM switch comprising:
a plurality of serial input ports coupled to a first bus;
a memory coupled to the serial input ports; and

a plurality of serial output ports coupled to the memory and to a second bus, wherein each serial input port and each serial output port are coupled to a programmable counter comprising:

multiple latches for providing a count output;

a start count circuit coupled to the latches;

a stop count circuit coupled to the latches; and

a compare circuit coupled to the stop count circuit and the latches that causes the latches to be reset based on the count output and values provided by the stop count circuit.

20. (Previously Presented) The ATM switch of claim 19 and further comprising a controller coupled to the ATM switch for controlling routing of ATM cells of data between serial input ports and serial output ports.

21. (Previously Presented) The ATM switch of claim 19, wherein each of the serial input ports and the serial output ports are double buffered.

22. (Currently Amended) A switch comprising:

a plurality of input ports coupled to a first bus;

a memory coupled to the input ports;

a plurality of output ports coupled to the memory and to a second bus, wherein each input port and each output port are coupled to a programmable counter having programmable start and stop values the programmable counter counting from zero to a maximum and programmed to increment the start value until the start value reaches the maximum at which time the start value rolls over the start address to the zero and continues to increment the start value until it reaches the stop value ; and

a controller coupled to the ATM switch for controlling routing of cells of data between input ports and output ports.

23. (Previously Presented) An ATM switch comprising:

a plurality of serial input ports coupled to a first bus;

a memory coupled to the serial input ports;

a plurality of serial output ports coupled to the memory and to a second bus;

a parity generator coupled between the serial input ports and the memory;

a parity checker coupled between the memory and the serial output ports;

a controller coupled to the ATM switch for controlling routing of cells of data between serial input ports and serial output ports; and

wherein each serial input port and each serial output port are coupled to a programmable counter comprising:

multiple latches for providing a count output;

a start count circuit coupled to the latches;

a stop count circuit coupled to the latches; and

a compare circuit coupled to the stop count circuit and the latches that causes the latches to be reset based on the count output and values provided by the stop count circuit.

24. (Previously Presented) The ATM switch of claim 23, wherein each of the serial input ports and the serial output ports are double buffered.

25. (Previously Presented) An ATM switch comprising:

a plurality of serial input ports coupled to a first bus;

a memory coupled to the serial input ports; and

a plurality of serial output ports coupled to the memory and to a second bus, wherein each serial input port and each serial output port are coupled to a programmable counter comprising:

multiple latches for providing a count output, wherein the latches further comprise circuitry for resetting the value of the count output to the start value upon reaching the stop count;

a start count circuit coupled to the latches;

a stop count circuit coupled to the latches; and

a compare circuit coupled to the stop count circuit and the latches that causes the latches to be reset based on the count output and values provided by the stop count circuit.

26. (Previously Presented) The ATM switch of claim 25 and further comprising:
a parity generator coupled between the serial input ports and the memory; and
a parity checker coupled between the memory and the serial output ports.

27. (Previously Presented) The ATM switch of claim 25 and further comprising a controller coupled to the ATM switch for controlling routing of ATM cells of data between serial input ports and serial output ports.

28. (Previously Presented) The ATM switch of claim 25, wherein each of the serial input ports and the serial output ports are double buffered.

29. (Previously Presented) An ATM switch comprising:
a plurality of serial input ports coupled to a first bus;
a memory coupled to the serial input ports; and
a plurality of serial output ports coupled to the memory and to a second bus, wherein each serial input port and each serial output port are coupled to a programmable counter comprising:
multiple latches for providing a count output;
a start count circuit coupled to the latches;
a stop count circuit coupled to the latches;
a maximum count circuit coupled to the latches, wherein the maximum count circuit includes a toggle controller for receiving the count output and selectively providing toggle control signals to inputs of the latches; and
a compare circuit coupled to the stop count circuit and the latches that causes the latches to be reset based on the count output and values provided by the stop count circuit.

30. (Previously Presented) The ATM switch of claim 29, wherein the toggle controller is provided the count output from the latches and further provides a toggle control signal to each

latch causing each latch to generate a 0 bit count based on a predetermined rollover value of the count output.

31. (Previously Presented) The ATM switch of claim 30, wherein the rollover value of the count output is decimal 111.

32. (Previously Presented) The ATM switch of claim 29, wherein the latches further comprise circuitry for resetting a value of the count output to a start value upon reaching a stop count.

33. (Previously Presented) A method for counting packets of cell data on a switch, the method comprising:

limiting a switch count to a switch maximum count value;

providing a switch start count value;

providing a switch stop count value that may be less than the switch start count value;

counting sequentially from the switch start count value;

resetting the switch count upon reaching the switch maximum count value;

continuing to count until the switch stop count value is reached; and

resetting the switch count to the switch start count value upon reaching the switch stop count.

34. (Previously Presented) The method of claim 33, wherein the method is performed in an order recited in claim 33.

35. (Previously Presented) A method for transferring packets of ATM cell data on an ATM switch, the method comprising:

limiting a switch count to a switch maximum count value of decimal 111;

providing a switch start count value;

providing a switch stop count value that may be less than the switch start count value;

counting sequentially from the switch start count value;

transferring one or more bits of ATM cell data from an input port to an output port;

resetting the switch count upon reaching the switch maximum count value;

continuing to count until the switch stop count value is reached; and

resetting the switch count to the switch start count value upon reaching the switch stop count.

36. (Previously Presented) The method of claim 35, wherein the method is performed in an order recited in claim 35.